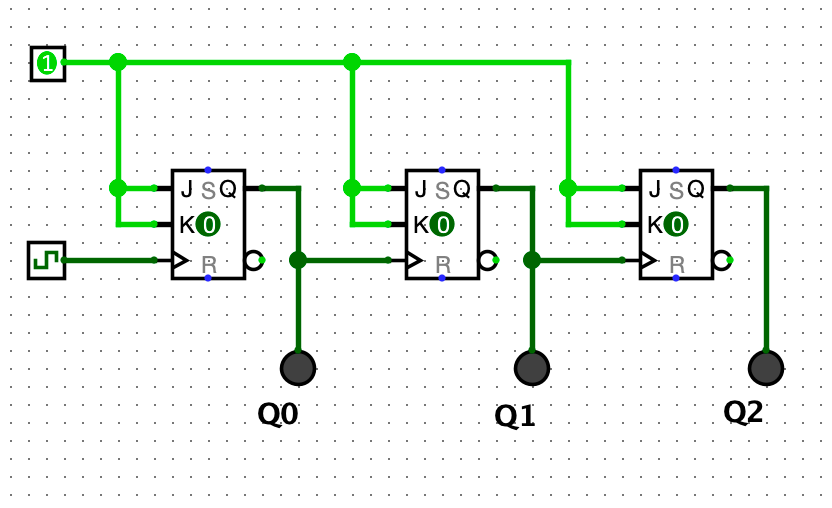
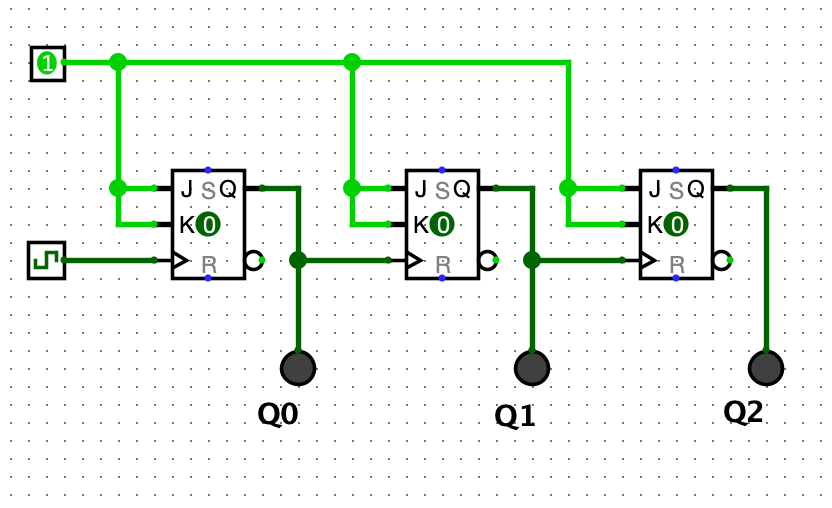
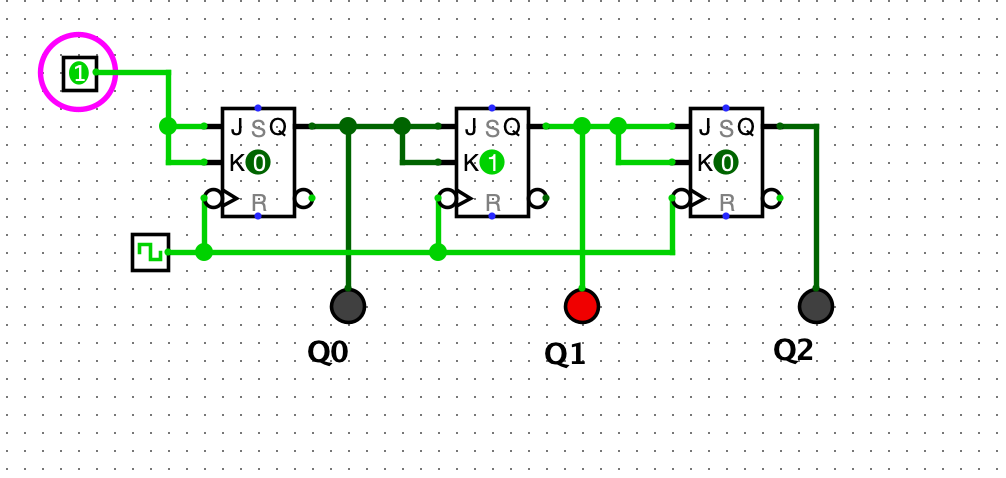
1. The most significant bit is going to be the one furthest away from the clock ( the last output ) State changes ripple through from least significant FF

**3-bit ripple counter ( FF Trigger set to Falling Edge )**

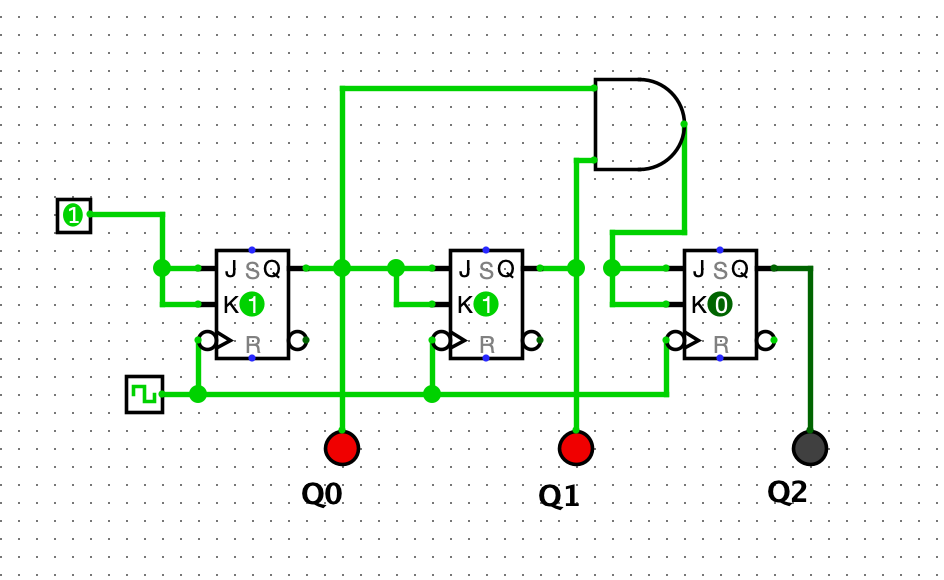


**3-bit count down counter ( FF Trigger set to Rising Edge )**

**0** **to 111**

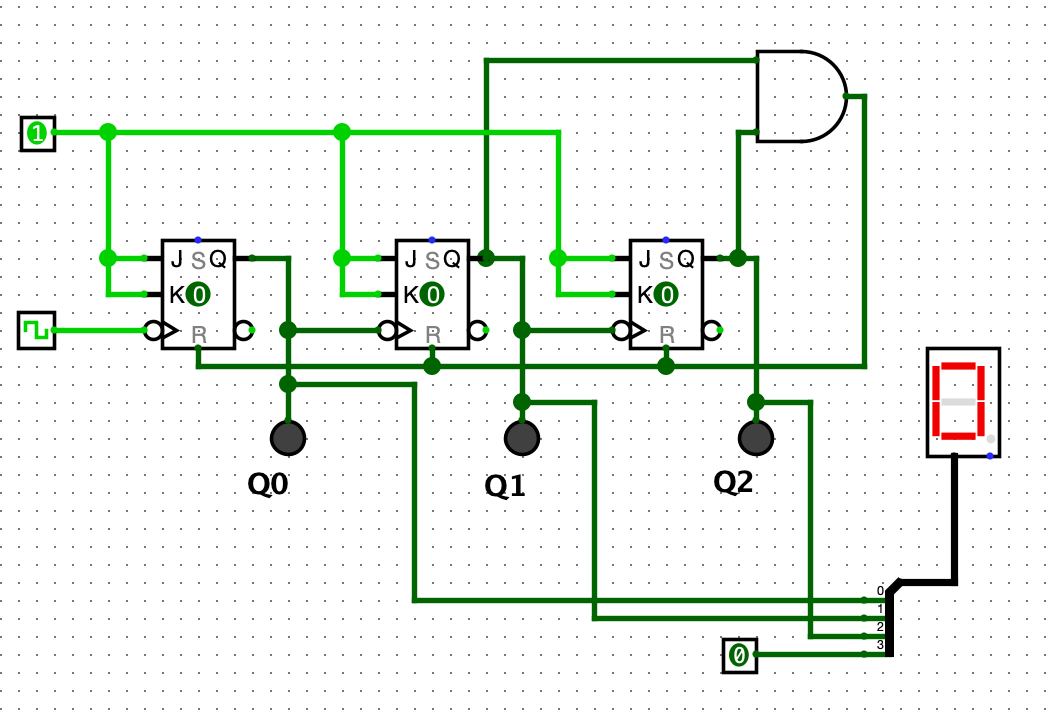
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**Momentary Illegal State**

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**Why is handling such things important?**

Because by using D FFs, it can buffer output for a clock pulse and allows circuit to stabilise. Also, illegal state cannot “escape”

**Finished Circuit**